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Performance Comparison of Positive Feedback Match-Line (ML) Sensing Schemes for Low Power TCAM

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Abstract: This paper presents a comparative performance analysis among different positive feedback based match line (ML) sensing scheme such as Mismatch dependent, Active feedback and Resistive feedback scheme. The comparison has been done based on parameters like search time, voltage margin, peak dynamic power and worst case energy consumption. Although most popular ML sensing scheme Current Race (CR) consumes more power than positive feedback based ML sensing scheme but performance comparison has also been shown between CR with each of three positive feedback based match line (ML) sensing scheme for equal search time. Finally, for search time Resistive feedback, for voltage margin and peak dynamic power consumption Mismatch dependent and for worse case energy consumption Active feedback scheme were found to be showing the best performance. For performance comparison the all the circuits is simulated using 130nm 1.2V CMOS logic.

Keywords: Ternary Content Addressable Memory (TCAM), positive feedback, Match Line Sensing Amplifier (MLSA), match line sensing scheme, current variation.

I. INTRODUCTION

In the era of modern data communication and networking, massive increase of internet users throughout the world has given birth to the demand of high speed internet networks. The internet network comprises of routers and switches which processes the data packets and sends it to an appropriate recipient. A header, user data and a trailer makes a data packet. In the header field there are flag, address field and control field [1]. When independent networks and links are connected to create internetworks (network of networks) or a large network, the connecting device (called routers or switches) route or switch the packets to their final destination [1]. The packets sent by the host computer may pass through numerous routers and switches before reaching the client computer. For this level of communication, we need a global addressing scheme; called Internet Protocol (IP) address in the network layer of the TCP/IP protocol suite.

Present internet protocol (IP) packet forwarding and classification performed in network routers and switches require high speed search capability to decide which action to be taken on the packet. Routers extract the information (such as destination address) contained in the packet header and search a table called routing table to find the most suitable match. Though software based search techniques are available, these are inherently slow as several instructions need to be executed and multiple memory accesses to external RAM are required to find a match [2]. Ternary content-addressable memory (TCAM) offers a high speed hardware solution to this problem [2]. TCAM can compare an input search data against a table of stored data and can return the address of the matching data in a single cycle. It can store don't care values which may result in multiple matches. The most suitable match is selected by a priority encoder. This makes TCAM even more attractive for network applications because of the requirement of finding the longest prefix match i.e. match with the entry having the fewest don't care values[3].

Generally a TCAM cell comprises of two SRAM cells and a comparator circuit. A single SRAM cell is constructed by two cross coupled inverter and 6 transistors are there in a single SRAM cell. The comparator circuit is made of 4 transistors. So, a TCAM cell is actually a 16-T structure shown. Match Line (ML), Search Line (SL) & Word Line are connected to a TCAM cell. Both NAND and NOR versions of comparison logic are popular for TCAM. But the NOR type comparison logic, has some advantages over NAND type and hence is more prevalent [2]. A detailed circuit diagram of TCAM is shown in Fig. 1.

This paper has been divided into five sections. Section II gives the idea of different match line sensing schemes. Section III describes the different methods of match line sensing when there is a positive feedback given in MLSA. Simulations results and performance analysis are

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illustrated in section IV. Conclusion is summarized in section V.

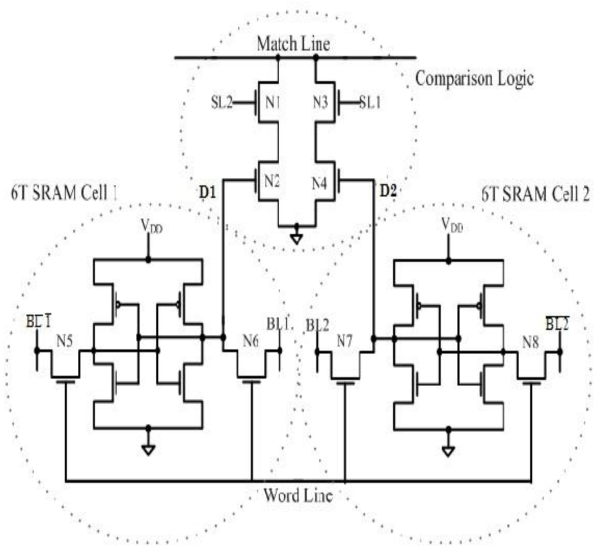

Fig. 1. Ternary Core cells for NOR- type CAM [3]

II. MATCH LINE SENSING SCHEME

In this section several match line sensing schemes and their procedure to generate the match result will be discussed.

A. Conventional (Precharge-High) Match Line Sensing

The basic scheme for sensing the state of the NOR match line is first to precharge high the match line and then evaluate by allowing the NOR cells to pull down the match lines in the case of a miss, or leave the match line high in the case of a match. The signal timing is divided into three phases: SL precharge, ML precharge, and ML evaluation. The operation begins by prechargeing the search lines low, disconnecting all the pull down paths in the NOR cells. With the pull down paths disconnected, the operation continues by asserting to precharge the match line high.

However the main problem associated with the conventional (prechage high) scheme is the energy consumption. All the MLs are precharged high first and then it remains high in case of match and discharged in case of mismatch. Usually, the number of match is very less compared to the number of mismatch. So a lot of energy is wasted during the detection of match or mismatch.

B. Low Swing Scheme

One method of reducing the ML power consumption, and potentially increasing its speed, is to reduce the ML voltage swing [4], [5]. In the case of a miss, the match line discharges through the CAM cell(s) to ground, whereas in the case of match, the match line remains at the precharge level.

A similar charge-sharing match line scheme was also described in [6]. But the trade-off here is the reduction of noise margin and area increment arising from the extra capacitor.

C. Selective Prechage Scheme

In conventional match line sensing scheme same power was allocated to the all the MLs and thus huge energy was wasted, regardless of the specific data pattern, and whether there is a match or a miss. We now examine three schemes that allocate power to match lines non-uniformly.

Selective precharge, performs a match operation on the first few bits of a word before activating the search of the remaining bits. For example, in a 32-bit word, selective precharge initially searches only the first 3 bits and then searches the remaining 29 bits only for words that matched in the first 3 bits. Assuming a uniform random data distribution, the initial 3-bit search should allow only 1/2 words to survive to the second stage saving about 88% of the match line power.

Selective precharge is perhaps the most common method used to save power on match lines [6], [7]–[11] since it is both simple to implement and can reduce power by a large amount in many CAM applications.

D. Pipelining Match Line Sensing Scheme

While the selective precharge scheme divides ML into two segments, pipelining scheme divides ML into more segments and perform comparison serially segment by segment [12], [13]. But both of the schemes energy saving depends on the data storage pattern and in worst case scenario there may be no energy saving. Again to do some initial matching some additional circuitry is used here which gives rise to more complexity.

The drawbacks of this scheme are the increased latency and the area overhead due to the pipeline stages. By itself, a pipelined match line scheme is not as compelling as basic selective precharge; however, pipelining enables the use of hierarchical search lines, thus saving power. Another approach is to segment the match line so that each individual bit forms a segment [14]. Thus, selective precharge operates on a bit-by-bit basis.

In this design, the CAM cell is modified so that the match evaluation ripples through each CAM cell. If at any cell there is a miss, the subsequent cells do not activate, as there is no need for a comparison operation. The drawback of this scheme is the extra circuitry required at each cell to gate the comparison with the result from the previous cell.

E. Current Race Scheme

The ML sensing schemes discussed so far suffers from different types of problem. For example: energy consumption is the most severe problem in conventional ML sensing scheme, low voltage margin and increased

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silicon area consumption is the main problem in low-swing scheme and complexity and worst case energy consumption is the main problem in selective precharge and pipelining ML sensing scheme respectively. So far most popular energy reduction scheme is Current Race (CR) scheme shown in Fig. 2.

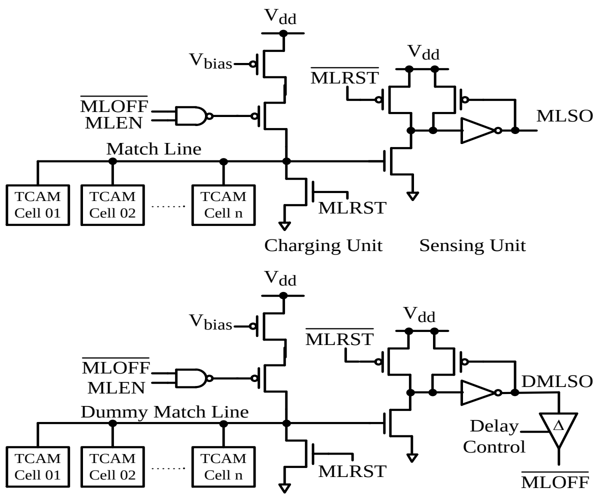

Fig. 2. Current Race scheme [3]

Unlike conventional ML sensing scheme MLs are pre-discharged to ground in CR scheme. MLEN signal initiates the search operation. During the search period MLs are charged towards high in case of match. SLs are not pre discharged to ground in this technique. This reduces the SL switching activity compared to the conventional scheme [3] and saves around 50% SL energy. For fully matched words the corresponding MLs get quickly charged to a threshold which causes the sensing unit to output high at MLSO. For mismatched words, MLs have discharging paths to ground, hence cannot be charged up to that threshold. So, outputs of the associated MLSAs remain low.

Both matched and mismatched MLs are given same current during the ML charging phase initially in CR scheme and current increases with increase in no of bits mismatching with the search data. It is evident from the simulation results that; current is the least in case of full match and its increasing with the number of bits mismatch. So, large amount of energy is wasted in large number of mismatched MLs in this scheme also.

III. MATCH LINE SENSING SCHEME WITH POSITIVE FEEDBACK IN MLSA

The main problem in CR scheme was that, the current given to both matched and mismatched MLs was same hence energy consumption was in higher side. We can reduce the power consumption by giving less current to the mismatched MLs compared to the matched MLs. This is one by using positive feedback in MLSA. Some positive feedback based scheme will be discussed in this section.

A. Mismatch Dependent Match Line Sensing Scheme

A general architecture for the Mismatch Dependent (MD) Match line Sensing scheme is shown in Fig. 3. The CAM array consists of a search-word register, which holds an n-bit search word, and m memory rows that store the CAM entries being searched. Also included in the array is a dummy row, which is designed to mimic a matched word. To save current, a current-saving control (CSC) block on each ML (Fig. 3) is included to monitor the voltage development on an ML and accordingly reduce the charging current as it becomes evident with time if an ML is mismatched [15].

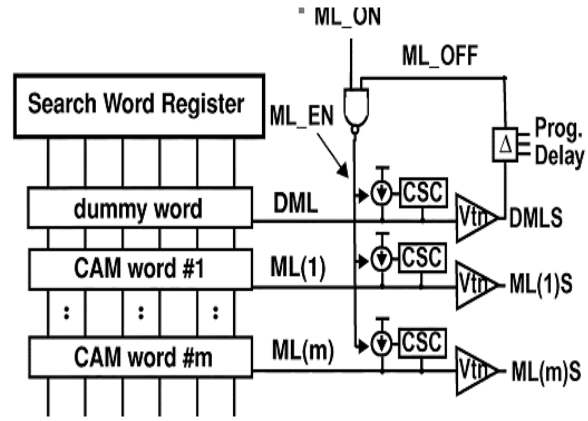

Fig. 3. Mismatch Dependent Match line Sensing Scheme [15]

The mismatch dependent (MD) MLSA in [15] suffers from the problem that, when idle, there is a dc path from Vdd to ground causing static power consumption.
Circuit diagram for this scheme in shown in Fig. 4.

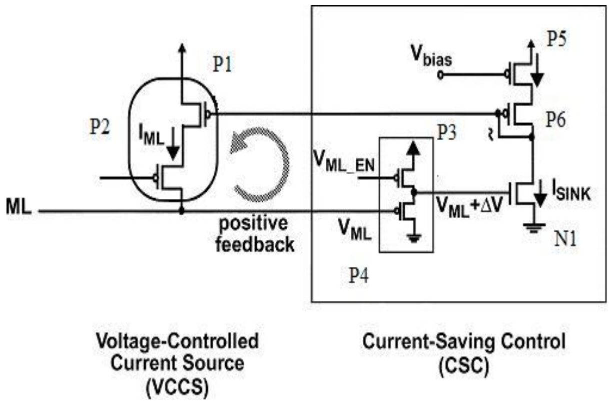

Fig. 4. Circuit level implementation of mismatch dependent ML sensing scheme [15]

B. Active Feedback Scheme

In order to reduce the energy consumption and delay without sacrificing the voltage margin, there is another positive feedback based ML sensing scheme called active feedback. The active feedback (AF) MLSA in [16] overcomes the problem in mismatch dependent scheme by redesigning the charging unit. The circuit diagram of active feedback scheme is shown in Fig. 5.

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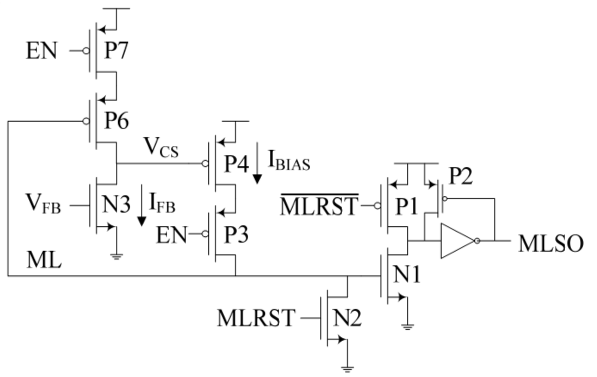

Fig 5 Circuit level implementation of Active Feedback ML sensing scheme [1]

C. Resistive Feedback Scheme

In addition to proposing active feedback MLSA, [16] introduced the concept of feedback with resistive shielding using an nMOS transistor in the charging unit of non-segmented ML. The transistor was operated in resistive region by a constant gate voltage.

A modified design [3] using an nMOS transistor with variable gate voltage and adjusting the gate dimensions of this transistor and the charging pMOS transistor in the first ML segment charging path. The nMOS transistor in [3] scheme operates in saturation region and its varying channel resistance acts as the feedback element only in the first segment MLSA. This modification results in less routing complexity and elimination of one extra analog voltage signal at the gate. Fig. 6 shows resistive feedback scheme

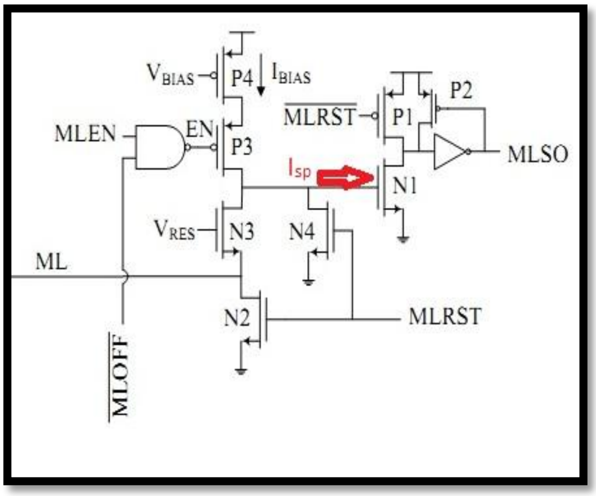

Fig. 6 Circuit level implementation of Resistive Feedback ML sensing scheme [1] [16]

IV. SIMULATION RESULTS & PERFORMANCE ANALYSIS

In this paper we have shown quantitative analysis among three types of match line sensing scheme with positive feedback in MLSA. Other studies such as [2], illustrated only the theoretical knowledge of those scheme. But in our paper we have shown the simulation results of those schemes for various parameters. So it becomes easy to use the better scheme as needed considering the values of those parameters. In our simulation we have used 130 nm & 1.2V CMOS technology for HSpice simulation. TCAM actually works in the form of array i.e. multiple words × multiple bits. In our simulation, we have used 32-words×32-bits TCAM arrays and a dummy word of same bit. We have performed comparative analysis among positive feedback based match line sensing scheme (Mismatch dependent, Active feedback, Resistive feedback) with Current Race match line sensing scheme. We have used CR as a reference design as it is tunable in a wide range of speed and compare the several parameters with it. Although there are a lot number of parameters, we worked only on search time, voltage margin, peak dynamic power and worst case energy consumption. For the sake of fair comparison we have tuned CR in three different cases in such a way that the search time of CR is fully matched with the search time of Mismatch Dependent, Active Feedback and Resistive Feedback respectively and then compared the voltage margin, peak dynamic power and worst case energy among them.

A. Match Line Current Variation

In case of feedback schemes full matched ML current will be highest and the current will be decreasing with the increase of number of bits mismatches.

In mismatch dependent sensing scheme Vbias was .6v and the minimum length and width, Lmin and Wmin are minimum feature size (130nm).

Simulation result of match line current variation in mismatch dependent scheme is shown in Fig. 7.

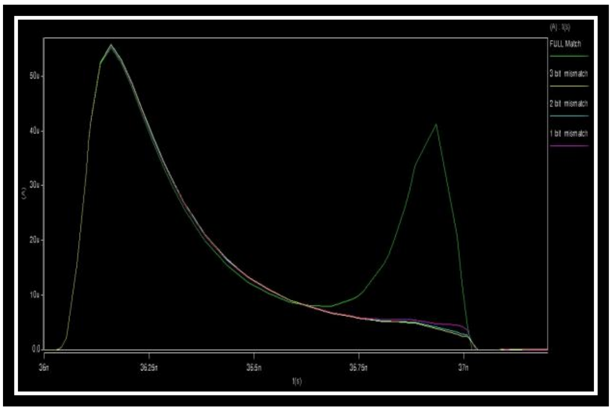

Fig7 ML current variation in mismatch dependent scheme

In case of current race scheme, the scenario is quite opposite. ML current is lowest in case of match and ML current increases with the increment of number of mismatch (Fig. 8). As the number of mismatches is generally higher in real time searching so the power consumption is on higher side in CR scheme and to reduce the power consumption the CR based positive feedback schemes were developed. All the feedback based schemes

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show similar results in ML current variations compared to the ML current variation in CR scheme.

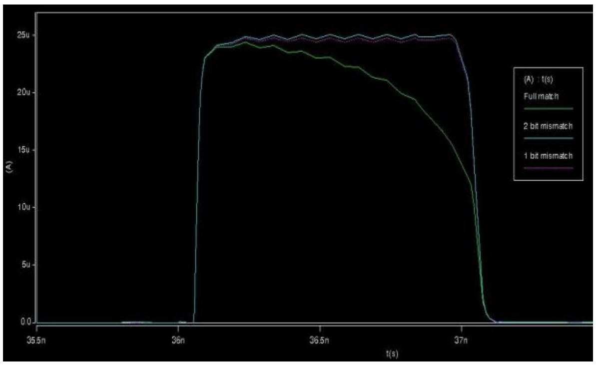

Fig. 8. ML current variation in current Race scheme

In active feedback scheme VFB was tuned to 0.55 and Lmin and Wmin are minimum feature size (130nm). Simulation result shows the behaviour of match line current variation in active feedback scheme is shown in Fig. 9.

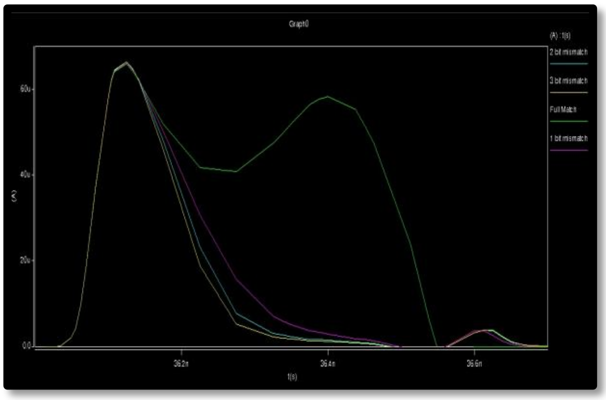

Fig. 9. Current Variation in active feedback ML sensing scheme

VRES was tuned to 0.76, Vbias was tuned 0.50 and Lmin and Wmin are minimum feature size (130nm).
The match line current variation in case of resistive feedback scheme is shown in Fig. 10.

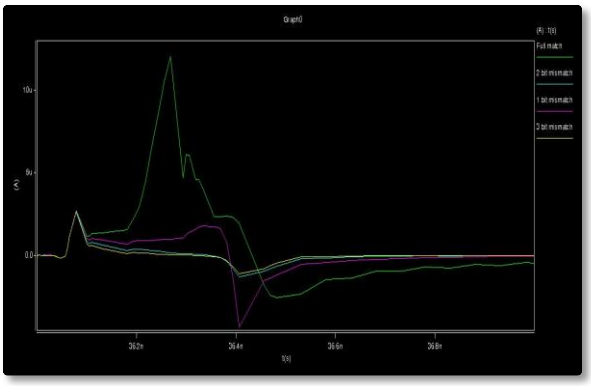

Fig. 10. Current Variation in resistive feedback ML sensing scheme

B. Search Time
Search time is defined as the time from 50% (0.6V) of MLEN to 50% (0.6V) of the final output of a matched ML (in case of 130 nm & 1.2 V logic) [3]. We found search time 738.99 ps for the mismatch dependent scheme for the circuit shown in Fig. 4.

In order to make comparison between MD scheme and CR scheme we tuned the gate parameters of CR in such a way that both MD and CR gives same search time that is 738.99 ps. Using the circuit shown in fig. 5 for active feedback sensing scheme we got the searching time 319.95 ps. For resistive feedback scheme we got the searching time 234.28ps. Fig. 6 is used for simulation.

C. Voltage Margin
Among all types of mismatches one bit mismatch causes maximum resistance in the ML pull-down path since there is only one path through which the ML can discharge. If there are multiple mismatches, multiple pull-down paths exist in parallel and hence the equivalent resistance of ML to ground path is lower which take less time for ML to discharge as the numbers of paths for discharging are increasing. Maximum resistance in the pull-down path means less charge leakage from ML to ground during match evaluation. Hence ML with 1-bit mismatch charges faster than MLs with more than one mismatch. So, 1-bit mismatch is the hardest to detect and it has the highest probability to be detected as a false match. So, there should be a distinct voltage gap between full match ML and 1 bit mismatch ML. Voltage margin is defined as the difference between the sensing threshold of the sensing unit and the maximum voltage to which a 1-bit mismatched ML is charged [3].
In case of mismatch dependent scheme (fig. 4) the voltage margin was 392.61 mV and equivalent speed CR has voltage margin 591.86mV. So from the above comparison we can say that CR has better voltage margin than same speed mismatch dependent sensing scheme.
In case of active feedback scheme (fig. 5) the voltage margin was 375.02 mV and equivalent speed CR has voltage margin 408.65mV. So from the above comparison we can say that CR has better voltage margin than same speed active feedback sensing scheme.
In case of resistive feedback scheme (fig. 6) the voltage margin was 378.28 mV and equivalent speed CR has voltage margin 268.7mV. So from the above comparison we can say that resistive feedback has better voltage margin than same speed CR sensing scheme.

D. Peak Dynamic Power and Worst Case Energy Consumption
Peak power consumption with worst case data pattern in routing table is a critical TCAM performance criterion. Many energy saving techniques concentrate on reducing average power consumption but the peak power consumption increases. Increased peak power consumption means more power has to be allocated for the TCAM chip which will be useful only for a short

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duration but during rest of the search cycle most of that allocated power remains unutilized. So, lower peak power consumption means cheaper supply can be used or the extra power can be used for other components. The worst case routing table used in energy comparison has been used to obtain peak power consumptions of various schemes.

In our simulation result the peak dynamic power of Mismatch dependent scheme was 2.4513 mW and CR was 1.53 mW. So in this case equivalent speed CR is better than mismatch dependent scheme. Again the worst case energy consumption of Mismatch dependent was 1074.85 fJ and CR was 1143.98 fJ. So if we move from the CR to MD we can save 6.04% of total energy. The peak dynamic power of active feedback scheme was 3.49 mW and CR was 3.189 mW. So in this case equivalent speed CR is better than active feedback scheme.

Again the worst case energy consumption of active feedback was 891.9 fJ and CR was 1370.4 fJ. So if we move from the CR to AF we can save 53.64% of total energy. The peak dynamic power of resistive feedback scheme was 3.533 mW and CR was 4.34 mW. So in this case resistive feedback is better than equivalent speed CR scheme. Again the worst case energy consumption of resistive feedback was 936.74 fJ and CR was 1581 fJ. So if we move from the CR to AF we can save 68.77% of total energy.

The comparison among the feedback schemes and equivalent speed CR is given below in table I, II, III.

TABLE I COMPARISON BETWEEN MD WITH EQUIVALENT SPEED CR

Comparison Parameter	**Mismatch Dependent scheme**	**Current Race of same speed**
Search Time (pS)	738.99	707.47
Voltage Margin (mV)	392.61	591.86
Peak dynamic Power (mW)	2.4513	1.58
Worst case energy consumption (fJ)	1074.85	1143.98

TABLE II COMPARISON BETWEEN AF WITH EQUIVALENT SPEED CR

Comparison Parameter	**Active Feedback**	**Current Race of same speed**
Search Time (pS)	319.95	325.56
Voltage Margin (mV)	375.02	408.65
Peak dynamic Power (mW)	3.49	3.189
Worst case energy consumption (fJ)	891.9	1370.4

TABLE III COMPARISON BETWEEN RF WITH EQUIVALENT SPEED CR

Comparison Parameter	**Resistive Feedback**	**Current Race of same speed**
Search Time(pS)	234.91	238.36
Voltage Margin (mV)	378.28	268.7
Peak dynamic Power (mW)	3.533	4.3460
Worst case energy consumption (fJ)	936.74	1581.00

The final comparison among the feedback schemes is shown in table IV.

TABLE IV COMPARISON AMONG MD, AF AND RF

Comparison Parameter	**Mismatch Dependent**	**Active Feedback**	**Resistive Feedback**
Search Time (pS)	738.99	319.95	**234.91**
Voltage Margin (mV)	**392.61**	375.02	378.28
Peak dynamic Power (mW)	**2.4513**	3.49	3.5334
Worst case energy consu-mption (fJ)	1074.85	**891.9**	936.74

Among the three positive feedbacks based scheme, resistive feedback is superior in term of search speed but it has a little bit degraded property in voltage margin, peak dynamic power and worst case energy consumption
In term of voltage margin and peak dynamic power mismatch dependent is superior although it is worst in term of search speed and worst case energy consumption.
In term of worst case energy consumption active feedback is superior and it is medium in search speed and peak dynamic power but worst in case of voltage margin.

V. CONCLUSIONS

We discussed three MLSAs that apply positive feedback for power reduction in ML sensing. Instead of providing the same current to all MLs, these MLSAs modulate the ML current source such that a larger current flows into the ML_0 (match) and a smaller current flows into the ML_K (mismatch).

In case of Mismatch dependant and active feedback scheme this energy saving comes in expense of reduced voltage margin and peak dynamic power. The worst case energy consumption is relatively less in these schemes compared to conventional CR-MLSA.

But the resistive feedback scheme shows no degradation of voltage margin and peak dynamic power compared to conventional CR-MLSA. Here also the worst case energy consumption is relatively less compared to conventional CR-MLSA.

We have found that among all three positive feedback based schemes resistive feedback provides with the best search time. The voltage margin and peak dynamic power is the best in case of Mismatch dependent scheme. Worst case energy consumption is least in Active feedback scheme among all three positive feedback based scheme.

So, our suggestion goes like this if the higher search speed is our main criteria then we must go for resistive feedback scheme. It the router is exposed to a noisy environment then we should go for the scheme which shows the best voltage margin which is the mismatch dependent scheme. If the energy consumption and heating of the device is of concern then we should opt for active feedback based scheme.

Future research can be carried out in understanding the search algorithms and applying that information to reduce the switching activity in SLs. In addition, innovative circuit techniques can be developed for the comparison logic to reduce the voltage swing and capacitance of SLs. Since large cell area is also a serious concern for large-capacity TCAMs, future research can also include the design of low-area TCAM cells that are compatible with the standard CMOS process. Non-volatile TCAMs can also be explored if the process technology supports the integration of high-speed logic and non-volatile memory.

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BIOGRAPHIES

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